Reviewed by: Devon Stedronsky

Module Name: Tx Priority Logic Requirements

Jira Ticket: CAN1-49

**CAN Controller Requirements Checklist Rev.2**

1. Is requirements document written clearly and grammatically correct?

Yes [x ] No [ ]

Comments:

1. Does requirements document define all functions to be performed by the module?

Yes [x ] No [ ]

Comments: *Specify i\_txempty values during state transitions.*

1. Does requirements document include all inputs and outputs to the module along with their corresponding accuracy, range of values, frequency and format?

Yes [x ] No [ ]

Comments:

1. Is each requirement unique?

Yes [ ] No [x ]

Comments: *Include ‘o\_send\_en’ and data values in each individual state requirements (TXPL\_16, 17)*

1. Does requirements document comply with system requirements and traceability?

Yes [ ] No [x ]

Comments: *Use specific system clock and CAN\_CLK signal names in TXPL\_2-5. Use specific signal name for internal state. Use specific internal signal name for latched value in TXPL\_12.*

1. Is terminology consistent with Requirements Standards?

Yes [x ] No [ ]

Comments:

1. Is it possible to implement all requirements?

Yes [x ] No [ ]

Comments:

1. Is each requirement testable or verifiable?

Yes [x ] No [ ]

Comments: *TXPL\_2, 3, 4 should be incorporated into the signal requirements or the state transition requirements. Not verifiable. Example; TXPL\_8: ‘o\_send\_en’ shall be set to 0 on the rising edge of ‘CAN\_CLK’ when ‘current\_state’ = idle.*